PATENT ABSTRACTS OF JAPAN

(11)Publication number : **07-273452**

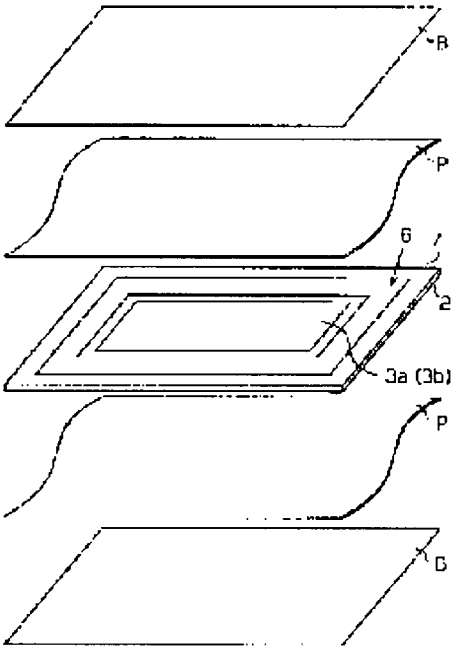
(43)Date of publication of application : **20.10.1995**

(51)Int.Cl. **H05K 3/46**

(21)Application number : **06-061614** (71)Applicant : **IBIDEN CO LTD**

(22)Date of filing : **30.03.1994** (72)Inventor : **NAGAYA FUMIJI**

(54) MULTILAYER PRINTED-WIRING BOARD AND MANUFACTURING METHOD THEREOF



(57)Abstract:

PURPOSE: To enable the finished thickness of the title printed-wirng board to be easily adjusted at a specific value without making a laminated layer test at all.

CONSTITUTION: The area of the conductor pattern including conductor circuits 3a, 3b is widened or narrowed by providing a board thickness adjusting pattern 7 on the surface whereon the conductor circuits 3a, 3b to be the inner layers of an insulating substrate 2 are formed. When the insulating substrate 2 and a prepreg P are used for lamination by widening or narrowing, the resin amount to be filled in the part excluding the conductor pattern of the insulating substrate 2 is fluctuated so as to adjust board thickness of the title multilayer printed-wiring board.

[Claim(s)]
[Claim 1]A multilayer printed wiring board which provided a pattern for board thickness adjustment for adjusting result board thickness of a multilayer printed wiring board in a field in which said conductor circuit of said insulating substrate is formed in a multilayer printed wiring board which laminated and carried out heat cure of an insulating substrate and prepreg in which a conductor circuit used as a inner layer was formed.
[Claim 2]A manufacturing method of a multilayer printed wiring board unified by hot press while laminating an insulating substrate characterized by comprising the following in which a conductor circuit used as a inner layer was formed via prepreg.
A value of result board thickness based on area of a conductor circuit at conditions that thickness of said conductor circuit and use number of sheets of said prepreg are certain.
It is a conductor circuit so that area of a conductive pattern according to a difference with a value of result board thickness for which it asks may be determined and the area may be set to 0.

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention relates to a multilayer printed wiring board and a manufacturing method for the same, and relates to the value of a request of the result board thickness after manufacture easily in detail at a multilayer printed wiring board which can be adjusted, and a manufacturing method for the same.
[0002]
[Description of the Prior Art]In recent years, densification of the printed wired board, i.e., multilayering of a printed wired board, is frequently performed with the miniaturization of electronic equipment, and high-density-assembly-izing of electronic parts.
[0003]As an element taken into consideration when designing a multilayer printed wiring board, there are the size of a board, a number of layers, a size of a hole, board thickness (total thickness), conductor width, conductor spacing, etc. Also in this, there is restriction that the diameter of the smallest through hole of the board thickness of a multilayer printed wiring board must be thinner than 3 times with regards to the size of holes, such as a plating through hole. That is, board thickness is set as the thickness which does not have influence in hydrodynamic movement, when immersed in copper or the plating liquid of solder. Therefore, when manufacturing a multilayer printed wiring board, it is required that the result board thickness according to the diameter of the through hole should be attained.
[0004]The lamination examination by arbitrary lamination is done as a method for obtaining desired result board thickness conventionally, and lamination is changed based on the test data, or he changes heating and a pressurizing condition, and is trying to adjust result board thickness.

[0005]In changing lamination, it is making change of the thickness of the inner layer insulating substrate which consists of glass epoxy resin etc. which include a conductor circuit, for example, change of the use number of sheets of prepreg, or a change of the resin content of prepreg.
[0006]In changing heating and a pressurizing condition, when result board thickness is thin, a pressure is lowered or application-of-pressure temperature is made high, for example, and in being conversely thick, a pressure is raised or it makes application-of-pressure temperature low.
[0007]And manufacture of a multilayer printed wiring board is performed based on the lamination, or heating and the pressurizing condition in the time of the result board thickness which repeats a lamination examination as mentioned above and is demanded being obtained.
[0008]
[Problem(s) to be Solved by the Invention]However, in the manufacturing method of the above-mentioned multilayer printed wiring board, after doing a lamination examination once, while having to change lamination etc., having to carry out by repeating a lamination examination once [at least] and taking time and effort, there is a problem of becoming the hindrance of shortening of production time.
[0009]When changing lamination and manufacturing a multilayer printed wiring board, it is necessary to prepare several prepregs from which several inner layer insulating substrates from which thickness differs, and a resin content differ. For this reason, the kind of material used increases and there is a problem that it takes time and effort to newly secure a storage place or to choose a required material. Since hardening follows especially prepreg at a high temperature, it must be kept in the place where a fixed temperature and humidity environment are ready, and the storage time is also about three months and a short period of time. Therefore, there is a problem that it being necessary not only to take care that the kind of prepreg increases to a storage place or a period for every kind of the but a manufacturing cost increases.
[0010]Since heating and the pressurizing condition at the time of manufacturing a multilayer printed wiring board increase while the conditioning takes time and effort when changing heating and a pressurizing condition, a hot press machine is made to work for every product units, and there is a problem of causing the fall of productivity. That is, if the product of a different kind also has the same heating and pressurizing condition when manufacturing a multilayer printed wiring board generally, he is trying to laminate simultaneously to the peak of the capability of a hot press machine. However, if conditions differ for every product, irrespective of the size of the quantity of a product, a pressing machine will be made to work once with one product, and productive efficiency will worsen.
[0011]Made in order that this invention may solve the above-mentioned problem, the purpose is to provide a multilayer printed wiring board which can be easily adjusted to the value of a request of the result board thickness

after manufacture without doing a lamination examination, and a manufacturing method for the same.

[0012]

[Means for Solving the Problem]In order to solve above-mentioned SUBJECT the invention according to claim 1, In a multilayer printed wiring board which laminated and carried out heat cure of an insulating substrate and prepreg in which a conductor circuit used as a inner layer was formed, a pattern for board thickness adjustment for adjusting result board thickness of a multilayer printed wiring board was provided in a field in which said conductor circuit of said insulating substrate is formed.

[0013]In a manufacturing method of a multilayer printed wiring board unified by hot press while the invention according to claim 2 laminates an insulating substrate in which a conductor circuit used as a inner layer was formed via prepreg, On conditions that thickness of said conductor circuit and use number of sheets of said prepreg are certain, area of a conductive pattern according to a difference of a value of result board thickness based on area of a conductor circuit and a value of result board thickness for which it asks is determined, and it was made to fluctuate area of a conductive pattern which includes a conductor circuit so that the area may be set to 0.

[0014]

[Function]In the invention according to claim 1, the area of a conductive pattern including a conductor circuit fluctuates by providing the pattern for board thickness adjustment in the field in which the conductor circuit used as the inner layer of an insulating substrate is formed. The resin amount with which the portion which is not a conductive pattern of an insulating substrate at the time of lamination with an insulating substrate and prepreg is filled up changes, and the board thickness of a multilayer printed wiring board is adjusted by the change in this area. Therefore, the result board thickness after manufacture is easily adjusted to a desired value by fluctuating the area of a conductive pattern with the pattern for board thickness adjustment corresponding to result board thickness and the area of the conductor circuit used as a inner layer, without doing a lamination examination.

[0015]In the invention according to claim 2, the thickness of a conductor circuit and the use number of sheets of prepreg on certain conditions. The area of the conductive pattern according to the difference of the value of the result board thickness based on the area of the conductor circuit and the value of the result board thickness for which it asks is determined, and the pattern for board thickness adjustment is provided in the increase in the area of the conductive pattern which includes a conductor circuit so that the area may be set to 0. And the result board thickness after manufacture is easily adjusted to a desired value, without doing a lamination examination.

[0016]

[Example]

(Example 1) Example 1 which materialized this invention is hereafter

described according to drawing 1 - drawing 3.

[0017]As shown in drawing 2, the voltage plane 3a and the earth layer 3b as a conductor circuit are formed in both sides of the insulating substrate 2, respectively, and the multilayer printed wiring board 1 has each class 3a and four layer systems by which the conductor circuit layers 5a and 5b were formed via the insulating layer 4 on 3b. The insulating substrate 2 consists of glass epoxy resin, and the insulating layer 4 is the same glass epoxy resin, and is formed by hardening of the prepreg used as adhesives at the time of manufacture of a multilayer printed wiring board.

[0018]As shown in drawing 1 and drawing 2, the voltage plane 3a and the earth layer 3b are formed in the small area rather than the outline area to both sides (only one side is illustrated in drawing 1) of the insulating substrate 2, and the agenesis field 6 of the conductor circuit is established in the circumference of each class 3a and 3b on the insulating substrate 2, respectively. The dummy pattern 7 for board thickness adjustment which consists of the same copper foil as the voltage plane 3a and the earth layer 3b is formed in each agenesis field 6, respectively. And the internal layer conductor pattern is formed with the voltage plane 3a and the earth layer 3b, and the dummy pattern 7. The dummy pattern 7 is formed in a predetermined area based on the relation between the result board thickness of a request of the multilayer printed wiring board 1, and the gross area of an inner layer conductor circuit. In this example, the gross area of an inner layer conductor circuit (the voltage plane 3a and the earth layer 3b) is called inner layer circuit area, and the gross area of an internal layer conductor pattern including a conductor circuit is called inner layer pattern area. And as for inner layer circuit area, inner layer pattern area is 70 cm^2 by 50 cm^2. The total area of both sides of the insulating substrate 2 is 100cm^2 (the sizes of a substrate are 10 cm x 5 cm).

[0019]Next, the manufacturing method of the multilayer printed wiring board 1 is explained. First, the relation between result board thickness and inner layer circuit area is explained. As shown in the graph of drawing 3, result board thickness has inner layer pattern area and a fixed relation, is finished by the change in the area, and also fluctuates board thickness. That is, at the time of manufacture of the multilayer printed wiring board 1, the thickness of the voltage plane 3a and the earth layer 3b and the use number of sheets of prepreg are certain conditions, and result board thickness changes with the quantity with which the portion which is not an inner layer pattern is filled up, when prepreg is in a flow state. Therefore, if board thickness becomes thick and decreases inner layer circuit area by forming the dummy pattern 7 and increasing inner layer pattern area, it will become thin. And the rate that board thickness changes becomes fixed according to the change in the inner layer pattern area formed in both sides of the insulating substrate 2.

[0020]In the above-mentioned relation, when the result board thickness made into the target (request) after lamination is set to 1.18 mm, an inner

layer pattern area required in order to obtain that target thickness is determined (in this case, 70cm^2). This inner layer pattern area the thickness of the inner layer copper foil which constitutes 0.6 mm, the voltage plane 3a, and the earth layer 3b for the thickness of the insulating substrate 2 70 micrometers, The thickness of 0.2 mm (0.1 mm x two sheets) and the copper foil B is asked for the thickness of the prepreg P which constitutes the insulating layer 4 before laminating with the relation between result board thickness when referred to as 18 micrometers, and inner layer pattern area. In this condition, as it is finished and board thickness is shown in drawing 3, inner layer pattern area changes from the board thickness (in this case, 1.09 mm) corresponding to 0 cm^2 at a rate that inner layer pattern area is constant to the board thickness (1.22 mm) corresponding to 100 cm^2.

[0021]Next, the difference of the internal layer conductor area (50cm^2) which doubled the actual voltage plane 3a and the earth layer 3b, and a required inner layer pattern area (70cm^2) is searched for (in this case, 20cm^2). That is, the determined area turns into area according to the difference of the value of the result board thickness based on the area of the voltage plane 3a and the earth layer 3b, and the target value of result board thickness. And the voltage plane 3a, the earth layer 3b, and the dummy pattern 7 are formed in both sides of the insulating substrate 2 for this area (20cm^2) with a conventional method as an area of the dummy pattern 7.

[0022]Then, after laminating where the 18-micrometer-thick copper foil B is inserted into the insulating substrate 2 via the prepreg P, carrying out hot press with a conventional method, forming a multilayer board and forming a through hole in the multilayer board, an outer layer conductor circuit is formed and the multilayer printed wiring board 1 is obtained.

[0023]As described above, in Example 1, the inner layer pattern area corresponding to target thickness is determined in the stage of a design pattern, and inner layer pattern area was adjusted for the difference with the inner layer circuit area of the inner layer pattern area and voltage plane 3a, and the earth layer 3b as a size of the dummy pattern 7. And after forming the dummy pattern 7 in both sides of the insulating substrate 2 simultaneously with the voltage plane 3a and the earth layer 3b, target thickness was obtained by laminating. Therefore, it can adjust to the value of a request of the result board thickness after manufacture of the multilayer printed wiring board 1 easily, without doing a lamination examination. The production time of the multilayer printed wiring board 1 can be shortened.

[0024]It becomes unnecessary to prepare several prepregs P from which several insulating substrates 2 from which thickness differs, and a resin content differ based on the test data of a lamination examination, or to change heating and a pressurizing condition. Therefore, the kind of the insulating substrate 2 or prepreg P can decrease, and the storage place of the material used can newly be secured, or the time and effort which chooses a required material can be saved. A manufacturing cost can be reduced while what is necessary is careful of a storage place or a period only to one kind of

prepreg P.
[0025]Since heating and a pressurizing condition are not changed, the product of a different kind can be simultaneously laminated by one set of a hot press machine, and causing the fall of productivity is lost.
[0026](Example 2), next Example 2 are described. In this example, when the inner layer pattern area corresponding to target thickness is determined, the area adjustment in the case of being smaller than the inner layer circuit area of the voltage plane 3a in which that inner layer pattern area is formed, and the earth layer 3b is explained.
[0027]For example, in the printed wired board which has the above-mentioned voltage plane 3a and the earth layer 3b, when the target thickness after lamination is set to 1.13 mm, an inner layer pattern area required in order to obtain that target thickness is determined first (in this case, $30cm^2$). Next, the difference of a actual inner layer circuit area ($50cm^2$) and a required inner layer pattern area ($30cm^2$) is searched for (in this case, $20cm^2$). And in order to remove this area ($20cm^2$) from the voltage plane 3a and the earth layer 3b, as shown in drawing 4, the opening K of two or more quadrangular shape is formed, and the conductive pattern of the mesh state that the gross area of each class 3a and 3b becomes 30 cm^2 is formed.
[0028]Therefore, even if smaller than the inner layer circuit area of the voltage plane 3a in which the inner layer pattern area corresponding to target thickness is formed, and the earth layer 3b, inner layer pattern area can be easily adjusted only by forming each class 3a and 3b in mesh state by the opening K, and target thickness can be attained.
[0029]Since the area of the voltage plane 3a and the earth layer 3b is small, when parts are mounted in the pad of an outer layer conductor circuit by solder reflow, heat becomes difficult to escape on each class 3a and 3b from a pad surface via a through hole (not shown). Therefore, parts can be soldered good.
[0030](Example 3), next Example 3 are described. This example explains area adjustment in case a inner layer is a signal plane which has not a solid pattern like the voltage plane 3a and the earth layer 3b but a wiring section.
[0031]As shown in drawing 5, the conductor circuit 8 is formed in both sides (only one side is illustrated) of the insulating substrate 2, respectively. The conductor circuit 8 has the composition that two or more wiring sections 10 which have the land 9 for through holes were arranged crosswise [of the insulating substrate 2]. The dummy pattern 11 which encloses each wiring section 10 with a prescribed interval is formed in both sides (only one side is illustrated) of the insulating substrate 2. This dummy pattern 11 is formed the approximately rectangular shape or the shape of L type in which the land 9 for through holes and the portion which counters were dented. And it is adjusted so that the area of the conductor circuit 8 may turn into inner layer pattern area corresponding to target thickness with the dummy pattern 11.
[0032]The above-mentioned dummy pattern 11 is formed based on the inner layer pattern area determined as follows. That is, inner layer pattern area

when the target thickness after lamination is 1.13 mm becomes 30 cm^2, as shown in drawing 3. When inner layer circuit area is 20cm^2, the conductive pattern in which inner layer pattern area includes the conductor circuit 8 of 30 cm^2 for 10 cm^2 area difference with inner layer pattern area as a size of the dummy pattern 11 is formed.

[0033]Therefore, a inner layer is a signal plane which consists of the conductor circuit 8, even if the inner layer circuit area is smaller than the inner layer pattern area corresponding to target thickness, by forming the dummy pattern 11, the inner layer pattern area to need can be adjusted and target thickness can be attained.

[0034]Although a part of wiring section 10 formed in the edge part side of the insulating substrate 2 at the time especially of etching melts easily, the wiring section 10 by the side of an edge part can be prevented from melting by enclosing the wiring section 10 with the dummy pattern 11.

[0035]This invention can also be materialized as follows.

(1) In Example 2, in addition to mesh state, as shown in drawing 6, the voltage plane 3a and the earth layer 3b, for example, Inner layer pattern area is adjusted, or the opening K of two or more small circle shape removes a part of voltage plane 3a and earth layer 3b, as shown in drawing 7, each neighborhood of the voltage plane 3a and the earth layer 3b is formed so that it may become ctenidium-like, and it may be made to adjust inner layer pattern area.

[0036](2) The dummy pattern 7 may be changed into copper foil, and it may form with resin, such as a solder resist.

(3) The insulating substrate 2 may be formed with a paper base epoxy resin, a synthetic-fiber-cloth substrate epoxy resin, paper base phenol resin, a woven glass fabric, a paper compound epoxy resin woven glass fabric, a nonwoven glass fabric composite base material epoxy resin, etc. The insulating layer 4 may be formed by the prepreg which consists of glass polyimide resin. There is an advantage that heat resistance improves in the case of glass polyimide resin.

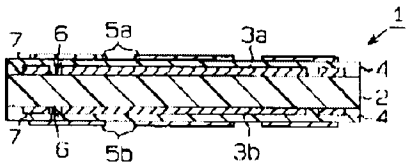
[0037](4) Although the dummy pattern 7 is formed in both sides of the insulating substrate 2 and inner layer pattern area was adjusted in Example 1, the dummy pattern 7 may be formed only in one side according to the size of the inner layer pattern area corresponding to result board thickness. In the multilayer printed wiring board 1 with which two or more voltage planes, earth layers, and signal planes were provided in the inner layer, Since what is necessary is just to adjust inner layer circuit area so that it may be finished and may become the inner layer pattern area corresponding to board thickness, a dummy pattern may be provided only about a voltage plane or an earth layer, or it may be made to delete a part. If it does in this way, inner layer pattern area can be adjusted easily.

[0038](5) In Example 1, the voltage plane 3a and the earth layer 3b, and the dummy pattern 7 may be formed in one. If it does in this way, a required inner layer pattern area can be easily obtained only by enlarging area of each

class 3a and 3b.
[0039](6) When making inner layer pattern area increase, it may be made to fatten the wiring section 10 in Example 3.
(7) The lamination of the multilayer printed wiring board 1 may be changed arbitrarily, or the thickness of the insulating substrate 2, the prepreg P used for lamination, the thickness of the copper foil B or the voltage plane 3a, and the earth layer 3b may be changed arbitrarily.
[0040](8) It may be made to form the outer layer conductor circuit of the multilayer printed wiring board 1 with an additive process, without using the copper foil B. The conductive pattern in this invention is defined as follows.
[0041]Conductive pattern: The figure or design of a conductive material formed on the insulating substrate or the insulating layer shall be said, and the solid pattern of the circuit pattern of a signal plane, a voltage plane, and an earth layer and dummy patterns other than this pattern shall be included in a multilayer printed wiring board.
[0042]The technical thought except having indicated to the claim which can be grasped from the above-mentioned example is indicated with the effect below.
(1) In the patchboard according to claim 1, as the wiring section of the conductor circuit formed in the edge part side of an insulating substrate in the pattern for board thickness adjustment was enclosed, it was provided. It can be made hard to melt in a wiring section at the time of etching, if it does in this way.
[0043](2) In the manufacturing method according to claim 2, when you needed deletion of the area of a conductive pattern and an inner layer conductor circuit was a solid pattern, the part was deleted. It can be made hard to escape from a pad surface to a solid pattern via a through hole in heat in the case of reflow soldering, if it does in this way.
[0044](3) In the patchboard according to claim 1, the wiring section which constitutes a conductor circuit for the pattern for board thickness adjustment was fattened, and it formed in one. If it does in this way, the area of a conductor circuit can be increased easily.
[0045](4) In the method according to claim 2, when making the area of a conductive pattern increase, the dummy pattern was formed in the agenesis field of a conductor circuit. If it does in this way, it is not necessary to change arrangement and shape of a conductor circuit and to secure the arrangement place of a dummy pattern.
[0046]
[Effect of the Invention]As explained in full detail above, according to claim 1 and the invention according to claim 2, it can adjust to the value of a request of the result board thickness of a multilayer printed wiring board easily, without doing a lamination examination.
[Brief Description of the Drawings]
[Drawing 1]It is an outline perspective view showing the lamination of the multilayer printed wiring board in Example 1 of this invention.

[Drawing 2]It is a type section figure showing a multilayer printed wiring board.
[Drawing 3]It is a graph which shows the relation between result board thickness and the gross area of an inner layer pattern circuit.
[Drawing 4]It is an outline top view showing the insulating substrate provided with the voltage plane of Example 2.
[Drawing 5]It is an outline top view showing the insulating substrate provided with the signal plane of Example 3.
[Drawing 6]It is an outline top view showing the insulating substrate provided with the voltage plane of other examples.
[Drawing 7]It is an outline top view showing the insulating substrate provided with the voltage plane of other another examples.
[Description of Notations]
1 [-- The earth layer as a conductor circuit, 4 / -- An insulating layer, 7, 11 / -- The dummy pattern for board thickness adjustment, 8 / -- A conductor circuit, 10 / -- A wiring section, P / -- Prepreg, K / -- Opening.] -- A multilayer printed wiring board, 2 -- An insulating substrate, 3a -- The voltage plane as a conductor circuit, 3b

【図2】



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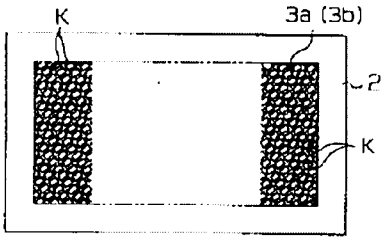
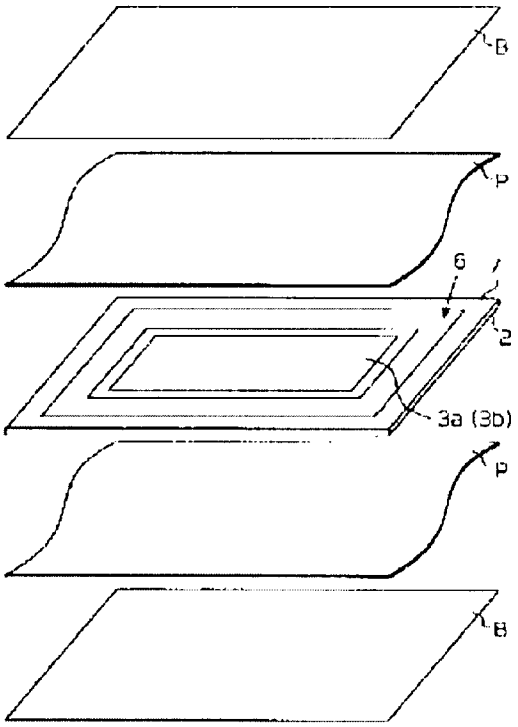


【図１】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6
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3a (3b)
P
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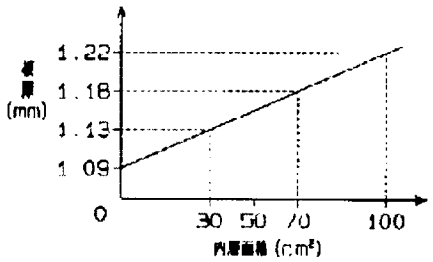
【図３】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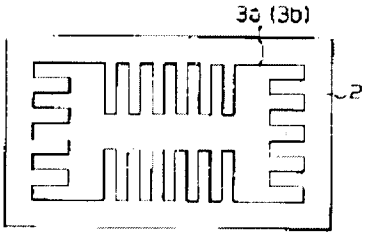
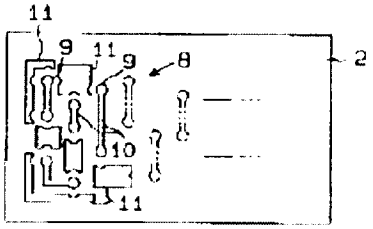

3a (3b)
2

【図５】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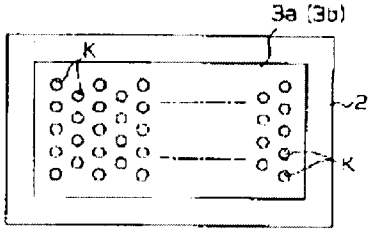
11

【図６】


3a (3b)
K
2
K